WHAT IS CLAIMED IS:

1. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate including at least one interconnect formed on the first semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the first semiconductor substrate; and

a second semiconductor substrate having at least one interconnect formed on the second semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged on the first semiconductor substrate and the first semiconductor substrate is arranged on the mount element such that a first main surface of the second semiconductor substrate rests on the first semiconductor substrate, and a first main surface of the first semiconductor substrate rests on the mount element, and wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

2. The semiconductor chip arrangement of claim 1 wherein the first and second semiconductor substrates each have an integrated circuit disposed in the area of the first main surface, wherein the integrated circuit is electrically coupled to the interconnect.

3. The semiconductor chip arrangement of claim 1 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

4. The semiconductor chip arrangement of claim 1 wherein the first main surface of the first semiconductor substrate is attached to the mount element.

5. The semiconductor chip arrangement of claim 1 wherein the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate.

6. The semiconductor chip arrangement of claim 1 wherein each of the first and second semiconductor substrates includes a dynamic random access memory formed therein.

7. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate arranged over the mount element, the first semiconductor substrate including at least one interconnect formed thereon, the first semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate;

a second semiconductor substrate arranged over the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect formed thereon, the second semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate, the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

a third semiconductor substrate arranged over the second semiconductor substrate, the third semiconductor substrate including at least one interconnect formed thereon, the third semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate, the third semiconductor substrate arranged so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate.

8. The semiconductor chip arrangement of claim 7 wherein the first, second and third semiconductor substrates each have an integrated circuit disposed therein, wherein the integrated circuit is electrically coupled to the interconnect.

9. The semiconductor chip arrangement of claim 7 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

10. The semiconductor chip arrangement of claim 7 wherein the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

11. The semiconductor chip arrangement of claim 7 wherein the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate.

12. The semiconductor chip arrangement of claim 11 wherein the contact area on the third semiconductor substrate extends to a first main surface on the third semiconductor substrate.

13. The semiconductor chip arrangement of claim 7 wherein each of the first, second, and third semiconductor substrates includes a dynamic random access memory formed therein.

14. A method for producing a semiconductor chip arrangement, the method comprising:

providing a mount element;

providing at least a first and a second semiconductor substrate, each of the first and the second semiconductor substrates having at least one interconnect and at least one contact area that is electrically connected to the respective interconnect, the contact area being arranged in a side surface of the respective semiconductor substrate;

placing the first semiconductor substrate on the mount element so that a first main surface of the first semiconductor substrate rests on the mount element; and

placing the second semiconductor substrate on the first semiconductor substrate such that a first main surface of the second semiconductor substrate rests on a second main surface of the first semiconductor substrate and an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate.

15. The method of claim 14 and further comprising, before placing either the first or the second semiconductor substrate, applying a conductive material locally to the contact areas of the first and the second semiconductor substrates.

16. The method of claim 14 and further comprising encapsulating the first and second semiconductor substrates.

17. A method for producing a semiconductor chip arrangement, the method comprising:

providing a mount element;

providing a first semiconductor substrate that includes at least one interconnect formed thereon and also includes at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate;

providing a second semiconductor substrate that includes at least one interconnect formed thereon and also includes at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate;

providing a third semiconductor substrate that includes at least one interconnect formed thereon and also includes at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate;

placing the first semiconductor substrate over the mount element such that a first main surface lies adjacent to the mount element;

placing the second semiconductor substrate over the mount element alongside the first semiconductor substrate such that a first main surface of the second semiconductor substrate lies adjacent to the mount element and such that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

placing the third semiconductor substrate over the second semiconductor substrate such that a first main surface of the third semiconductor substrate rests over a second main surface of the second semiconductor substrate, and such that an electrical contact is produced between the contact areas of the third semiconductor substrate and the contact area of the second semiconductor substrate.

1 18. The method of claim 17 wherein, before placing the semiconductor substrates, applying a
2 conductive material to the contact areas of the first, second, and third semiconductor substrates.

1 19. The method of claim 17 and further comprising encapsulating the first, second, and third
2 semiconductor substrates.